IN THE ABSTRACT:

Please replace the abstract as follows:

A disclosed semiconductor memory device ~~has~~ includes multilevel memory cells in which data in the cells is arranged according to a coding method that allows error correction.~~, each cell storing at least three levels of data each. At least a first data composed of first data bits and a second data composed of second data bits are arranged in order that at least a bit of an N-order of the first bits and a bit of the N-order of the second bits are stored in one of the cells, the N being an integral number. A voltage corresponding to the N-order bits is generated and applied to the one of the cells in response to an address information corresponding thereto. Another semiconductor~~ One disclosed device has multilevel memory cells arranged so as to correspond to a physical address space, each cell storing 2^n levels of data, each expressed by n ($n \geq 2$) number of bits (X1, X2, Xn). ~~A~~ When an input logical address is converted into a physical address ~~of the physical address space. Judging~~ , a determination is made whether ~~a~~ the logical address space ~~including the logical address~~ matches the physical address space. ~~When~~ If there is a matched, the most significant bit X1 is specified once using a reference value~~.~~, and ~~[[T]]~~the specified bit is output from one of the cells corresponding to the physical address. If there is not a matched, the bits (X2, ..., Xn) are specified by an n - time specifying operation ~~maximum~~ using maximum n number of different reference values. ~~The data writing/reading operations to/from the semiconductor devices can be stored in a computer readable medium as program codes for causing a computer to execute these operations.~~